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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,484	07/21/2003	Michael Setton	015290-755	4980

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EXAMINER

POMPEY, RON EVERETT

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/622,484

Applicant(s)

SETTON, MICHAEL

Examiner

Ron E. Pompey

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 September 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 38-47 and 49-52 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 40-43 is/are allowed.
- 6) ☒ Claim(s) 39-39 and 44-52 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 38-39 and 44-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfister (US 5,200,352) in view of Wu (5,880,508) in further view of admitted prior art or Ohiwa et al. (4,947,081).

Pfister discloses the limitations of:

forming an interfacial layer (14, fig. 1A), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate; and

forming a gate electrode of an electrically conductive material on the interfacial layer;

source and drain regions (32, fig. 1E) that are adjacent the gate electrode(col. 2, ln. 48 – col. 4, ln. 33); and

forming spacer (20, fig. 1A) adjacent to the gate electrode and on an upper surface of the interfacial layer (col. 5, lns. 30-41).

3. Pfister reads on the claims as applied above, but does not disclose the claimed limitation(s) below of:

forming a high dielectric constant layer (8, fig. 1) on the interfacial layer;

forming a high dielectric constant layer (2, fig. 5a) on the interfacial layer, the comprises a material that is selected from the group consisting of  $Ta_2O_5$ ,  $Ta_2(O_{1-x}N_x)_5$  wherein x ranges from greater than 0 to 0.6, a solid solution of  $(Ta_2O_5)_t - (ZrO_2)_{1-t}$  wherein t ranges from about 0.9 to less than 1, and a solid solution of  $(Ta_2O_5)_u - (HfO_2)_{1-u}$  wherein u ranges from about 0.9 to less than 1 and a solid solution  $(Ta_2O_5)_s - (Al_2O_3)_{1-s}$  wherein s ranges from 0.9 to less than 1 wherein the interfacial layer separates the high dielectric constant layer from the substrate;;

having a gate width of less than 0.3 micron covering the high dielectric constant layer; and

wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

However,

a. Wu discloses the above claimed limitations regarding:

forming a high dielectric constant layer (8, fig. 1) on the interfacial layer (6, fig. 1), the comprises a material that is selected from the group consisting of  $Ta_2O_5$ , wherein the interfacial layer comprises silicon nitride or silicon oxynitride;

wherein the interfacial layer separates the high dielectric constant layer from the substrate; and

having a gate width of less than 0.3 micron covering the high dielectric constant layer (column 1, ln. 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pfister with Wu, because the high dielectric constant

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layer provides for a gate insulator layer that reduces hot carrier effect; and the gate width of less than 0.3 micron take up less wafer real estate, which means more devices can be formed on one wafer. Note: that because the spacers are formed after the gate oxide in Pfiester the spacers would also be formed on the high dielectric layer when combining Wu with Pfiester.

b. Pfiester and Wu, fail to disclose the limitations of:

wherein the high dielectric layer comprises one of the following,  $Ta_2(O_{1-x}N_x)_5$  wherein x ranges from greater than 0 to 0.6. However the admitted prior art, on page 6, line 24 –26, or Ohiwa , column 2, lines 45-58, discloses that a high dielectric layer can be formed of the above compositions. Also, Ohiwa discloses that tantalum oxynitride in the claimed range is art recognized equivalent to tantalum pentoxide.

Also, in applicants' specification, page 7, line 25 – page 8 , line 3, states that it is conventional for photoresist/lithography techniques to form a gate pattern that will form the line width of a gate less than 0.3 micron.

Therefore it would have been obvious to one of ordinary skill in the art to combine the admitted prior art (APA) and/or Ohiwa with Wu, because the above listed materials are art equivalent high dielectric material with  $Ta_2O_5$  of the Wu reference.

***Allowable Subject Matter***

4. Claims 40-43 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singly or in combination, fails to disclose the limitations of: wherein the high dielectric layer comprises one of the following

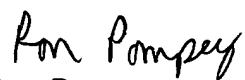
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compositions, a solid solution of  $(\text{Ta}_2\text{O}_5)_t - (\text{ZrO}_2)_{1-t}$ , and a solid solution of  $(\text{Ta}_2\text{O}_5)_u - (\text{HfO}_2)_{1-u}$  wherein  $t$  and  $u$  range from about .09 to less than 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Ron Pompey  
AU: 2812  
September 19, 2005

  
MICHAEL LEBENTRITT  
SUPERVISORY PATENT EXAMINER